REMARKS

The present Amendment amends claims 17, 18, 21-23, 27, 28, 31, 32 and 35-37 and leaves claims 19, 20, 24-26, 29, 30, 33, 34 and 38-40 unchanged. Therefore, the present application has pending claims 17-40.

Claims 17-40 stand rejected under 35 USC §103(a) as being unpatentable over DeGroot (U.S. Patent No. 4,766,564) in view of Chevillat (U.S. Patent No. 4,615,004). This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claims 17-40 are not taught or suggested by DeGroot or Chevillat whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to the claims to more clearly recite that the present invention is directed to a processor having a sequencer which causes a plurality of instructions at a time to be fetched from memory in one machine cycle, wherein the instructions use a plurality of arithmetic operation units in parallel, and a bypass circuit for operating the arithmetic operation unit to use data resulting from an operation by an arithmetic operation unit for a next cycle operation.

Thus, by use of the above described features of the present invention high speed arithmetic operations can be performed in a manner by executing multiple instructions in parallel where possible. Such features are clearly not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, these features of the present invention now more clearly recited in the claims are not taught or

suggested by DeGroot or Chevillat whether taken individually or in combination with each other as suggested by the Examiner.

DeGroot teaches a data processing system having multiple floating point arithmetic units including, for example, an adder and a multiplier. DeGroot teaches that the floating point arithmetic units are operated in parallel. However, there is no teaching or suggest in DeGroot of the fetching of a plurality of instructions at one time as recited in the claims. Particularly, there is no teaching or suggestion in DeGroot of the fetching of a plurality of instructions at a time, wherein the plurality of instructions use a plurality of arithmetic operation units as in the present invention. DeGroot merely teaches that one instruction is fetched at a time and the fetched instruction is selectively sent to one of the floating point arithmetic units such that a subsequent instruction is sent to the other of the floating point arithmetic units. As such it is quite clear that there is no teaching or suggestion in DeGroot of fetching plural instructions at a time so that the plural instructions being fetched use plural arithmetic operation units as in the present invention.

Thus, DeGroot fails to teach or suggest a sequencer which causes a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using a plurality arithmetic operation units as recited in the claims.

The above noted deficiencies of DeGroot are not supplied by any of the other references of record. Particularly, the above noted deficiencies of DeGroot are not supplied by Chevillat.

Chevillat discloses a microprocessor having a single arithmetic operation unit. The microprocessor taught by Chevillat fetches at one time a

LOAD/STORE instruction which does not use the arithmetic operation unit and an arithmetic instruction which uses the arithmetic operation unit. Thus, the fetching operation as taught by Chevillat is quite different from the present invention as recited in the claims.

Although, Chevillat and DeGroot also intend to speed up arithmetic operations, the processor of Chevillat is provided with one arithmetic operation unit and the distribution system can fetch only one instruction at a time. In contrast, according to the present invention a processor is provided with means for fetching at a time a plurality of instructions using a plurality of arithmetic units in parallel and a bypass circuit for operating the arithmetic units efficiently. Therefore, the present invention accomplishes high-speed arithmetic operation that could not be done by the references of record, namely Chevillat and DeGroot.

Thus, Chevillat fails to teach or suggest a sequencer which causes a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using a plurality arithmetic operation units as recited in the claims.

Further, Chevillat fails to teach or suggest a plurality of arithmetic operation units capable of executing the plurality of instructions fetched from the memory in parallel as recited in the claims.

Therefore, as per the above, both DeGroot and Chevillat suffer from the same deficiencies relative to the features of the present invention as now more clearly recited in the claims and as such when combined fail to teach or suggest the features of the present invention as recited in the claims.

Accordingly, reconsideration and withdrawal of the 35 USC §103(a) rejection of claims 17-40 is respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 17-40.

In view of the foregoing amendments and remarks, applicants submit that claims 17-40 are in condition for allowance. Accordingly, early allowance of claims 17-40 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (500.28166CX2).

Respectfully submitted,

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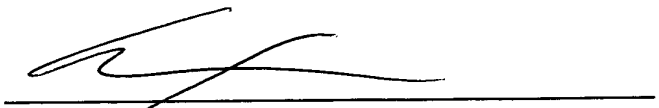

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